Synchronous Detection of DSB and ISB Signals

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Background

A Synchronous Detector designed with the use of an LM311 and an Analog Devices AD607. This is a very basic design. It functions as a product detector and when JMP2 is closed and JMP 1 is open, it functions fully synchronously locking to the 455 KHz I.F. provided at the input. The 455 KHz input should be pre-filtered to remove unnecessary noise from the signal so as to improve locking performance. This circuit has been tested with a Hammerlund SP-600, and it functions quite well with the I.F. out of this receiver connected to J1 of this circuit. Most of the testing has been done with the SP-600 in its 8 KHz position however, any of the passband selections work fine. The narrower the bandwidth selection the better rejection there is against unwanted adjacent channel interference. Additional I.F. selectivity can be had by filtering just the signal provided to U1 and not the I.F. sent to U2. This is not shown below but can easily be implemented. Further improvement could be had, by regenerating the carrier with a Phase Locked Loop such as the NE564. This is necessary for use on signals with marginal carrier signal or suppressed carrier. The loop filter designed for use with such a PLL would provide much greater rejection of unwanted adjacent channel noise. This is an experimental breadboard and is by no means a polished performer. It does afford the experimenter the opportunity to play with a configuration that can provide synchronous detection. Have Fun!

Theory of Operation

The signal applied to J1 is between 1 to 2 volts, rms and is hard limited by U1, LM311. The limiting is necessary to remove amplitude variations of the signal due to the modulation components present. It is only the carrier we want the Phase Locked Loop in U2 to lock-up to. U1 is configured as a zero crossing detector. R1 & R2 bias the input signal to half of VCC. R3 & R4 provide the reference voltage to the comparator, which will determine the switching point of the comparator. The output of U1 is pulled up to VCC so it provides an output which swings between VCC and ground (+4.5v). It is not recommended to apply greater than 4.5 volts to this circuit because of limitations in U2. Nominally the AD607 runs at as little as 3 volts and under no circumstances wants to run above 5 volts. 4.5 volts is fairly standard and can be gotten from a wall transformer or 3 AA batteries. The output signal of U1 is sent through a trim pot which will limit the amplitude of the PLL reference signal to about 0.5 volts at the FDIN input at pin 1of U2. This signal is also biased at one half of VCC with R10 & R11. The selection of C3 and these resistors is such to minimize any phase distortion caused by the input coupling of these components.

The input signal from J1 is also sent through a resistor network, which conditions the signal for suitability at the input of the product detector in the AD607. These detectors are basically doubly balanced mixers and the local oscillator differs for the two detectors by 90 degrees. The PLL in the AD607 basically takes the reference signal that was limited in U1 and provides a new signal, which is in phase and in quadrature to that reference signal for application to the product detectors as shown in the U2 block. The PLL also has a loop filter, which is optimized for 455

KHz, however I did not notice much difference in performance when this time constant was lowered by an order of magnitude. So I wouldn't be too concerned about this when running I.F.s below 2 MHz.

The detected baseband signal is present at pin 18 of U2 (IOUT), and Pin 17 (QOUT) along with other mixing components. These other components should be filtered and R13, C9, R14, & C8 are selected to filter the outputs with a minimum of phase distortion. If you are going to only utilize this detector as a DSB Detector, then the Quadrature output available is not necessary, and it need not be used for anything. Just pass the In-phase output to an audio amplifier auxiliary input for amplification.

## Independent Sideband Synchronous Detection

This circuit has been used to provide a source for detection of independent, upper, and lower sideband signals. Unless there is a carrier present with these signals, it cannot operate in the synchronous mode as configured. An independent sideband (ISB) signal can be detected with this detector by utilizing both outputs (IOUT, & QOUT) and passing them to a phase demodulation network. The principle is very much like phasing sideband modulation, but in reverse. The ISB performance of the detector when locked to a carrier was somewhat dissappointing. For some reason that I have not discovered yet, the detecotr will not demodulate ISB when locked to the incoming carrier. It will however demodulate ISB perfectly when a non-phase locked oscillator running near 455 KHz is applied to J2 and the jumper at JMP 2 is removed and JMP is shorted. For ISB detection an external audio phasing network is necessary.

For this to happen it is necessary to utilize wideband audio phase shift networks known as Allpass Filters coupled with doubly balanced mixers. This network is much like the DOME networks originally designed in the 50's. An Allpass Filter design (see http://home.worldnet.att.net/~wa1sov/technical/allpass/allpass.html) can be used or a Digital Signal Processor (DSP) implementing a FIR filter can be employed. The ladder was how I have debugged this design. The concept is pretty simple. If you realize that the IOUT signal contains both sidebands of the signal in phase with each other, and that the QOUT signal contains the sum of upper and lower sidebands 90 degrees out of phase with the IOUT, then with additional phase delay the upper and lower sidebands can be demodulated independently. The IOUT channel gets passed through one Allpass filter, which alters the phase of the signal, by +45 degrees. The QOUT signal is passed through another Allpass filter, which alters the phase of this signal, by -45 degrees. This leaves a net difference of 180 degrees between the IOUT and QOUT Phase processed signals. Adding the IOUT and the QOUT phase processed signals yields a cancellation of the lower sideband. However, the upper sideband remains at the output of this summation and at twice its original amplitude. Now the same two signal are also subtracted from each other in another network to obtain the lower sideband. The lower sideband is also at twice its original amplitude. Thus the lower sideband appears on one channel and the upper sideband would appear on the other channel when applied to the input of a Stereo amplifier. In order for this to work with any degree of opposite sideband rejection close attention to phase accuracy and amplitude matching are paramount. I have obtained without any special optimization of these circuits when using a DSP running a 256 point FIR Filter, opposite sideband rejections of 30 dB. Better can be obtained though through rigorous optimization. Stay tuned!

The signal demodulated does not have to be synchronous to detect signals independently. The system can be used with an external function generator, which is not phase coherent (free running) with the signal. It will function as an independent sideband product detector and Upper and Lower Sideband can be discerned well with this mode.

I hope this article has stirred some interest in this type of detection. Additionally, CQUAM AM Stereo can be demodulated with the I and Q outputs of this detector by simply summing to obtain one channel and differencing to obtain the opposite stereo channel. This does not require the Allpass phasing network described above. Jerry, WA2FNQ transmits the old QAM Stereo signal that can be demodulated using this technique. There are more developments in the works so check back often.

Stay Tuned!
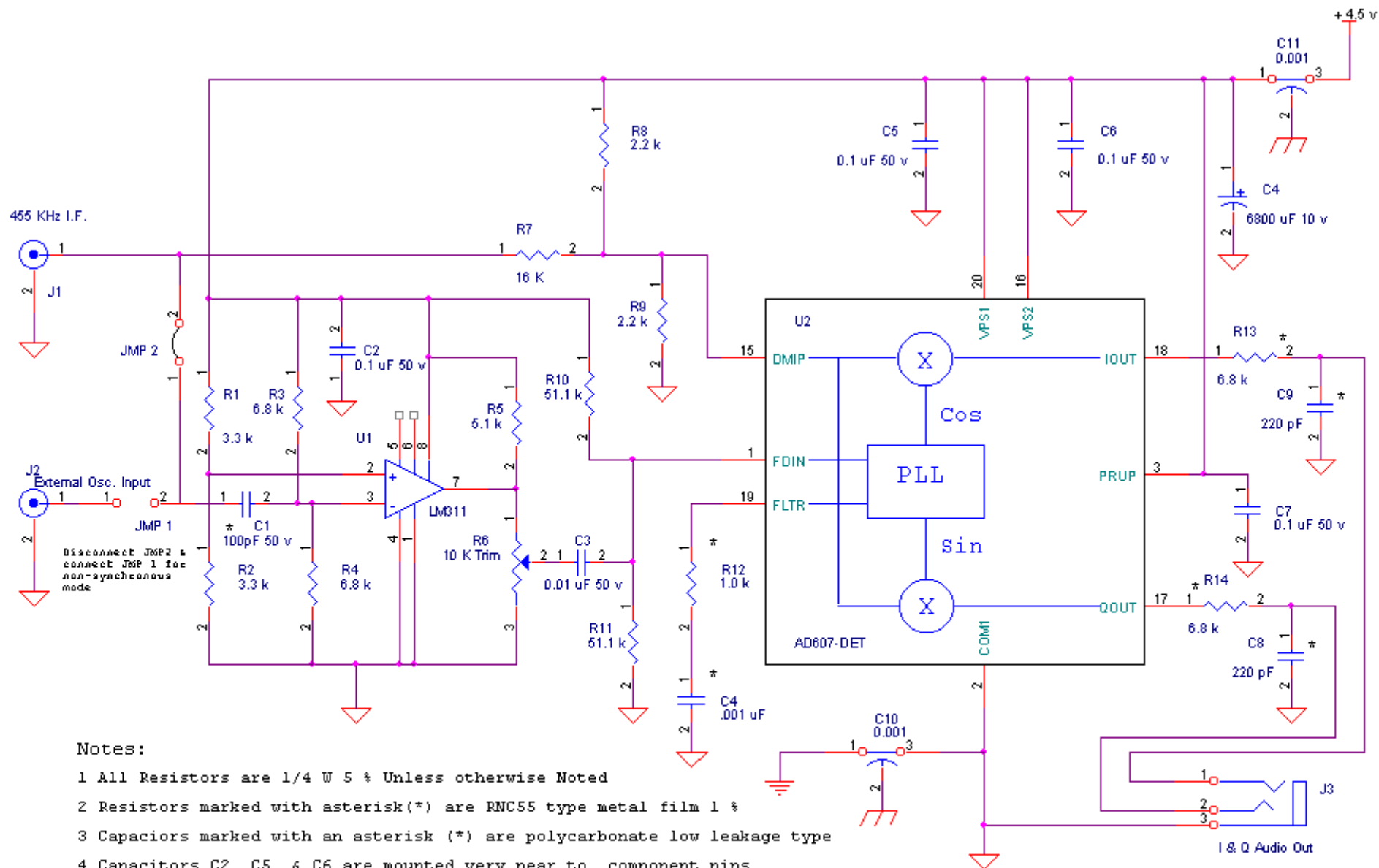
Notes:

1 All Resistors are 1/4 W 5 % Unless otherwise Noted

2 Resistors marked with asterisk(*) are RNC55 type metal film 1 %

3 Capaciors marked with an asterisk (*) are polycarbonate low leakage type

4 Capacitors C2, C5, & C6 are mounted very near to component pins

5 All interconnects should be kept as close as possible and circuitry should be layed out on a ground plane, and placed in a fully enclosed metal box with appropriate feedthough power bypasses.

455 KHz I.F.

J1

J2
External Osc. Input

JMP 1

JMP 2

Disconnect JMP2 & connect JMP 1 for non-synchronous mode

R1 / R3 6.8 k
3.3 k
R2 3.3 k
R4 6.8 k
C1 * 100pF 50 v
C2 0.1 uF 50 v
U1 LM311
R5 5.1 k
R6 10 K Trim
C3 0.01 uF 50 v
R7 16 K
R8 2.2 k
R9 2.2 k
R10 51.1 k
R11 51.1 k
R12 1.0 k
C4 .001 uF

+4.5 v

C11 0.001
C5 0.1 uF 50 v
C6 0.1 uF 50 v
C4 6800 uF 10 v

U2
AD607-DET
VPS1
VPS2
15 DMIP
Cos
X
PLL
Sin
1 FDIN
19 FLTR
X
COM1
IOUT 18
PRUP 3
QOUT 17

R13 * 6.8 k
C9 220 pF *
C7 0.1 uF 50 v
R14 * 6.8 k
C8 220 pF *

C10 0.001

J3
1
2
3
I & Q Audio Out

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Title	Synchronous Detector		Rev
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