Frequency-Selective AM Detection Using Monolithic Phase-Locked Loops

Application Note

INTRODUCTION

This application note describes the use of monolithic phase-locked loop (PLL) circuits in detection of amplitude-modulated (AM) signals. The detection capabilities of a PLL system, which is a frequency-selective FM demodulator, can be extended to cover AM signals simply by the addition of an analog multiplier (or mixer) and a low-pass filter to the basic phase-locked loop. This technique of AM demodulation, which is called synchronous AM detection, offers significant performance advantages over conventional peak-detector type AM demodulators, in terms of its dynamic range and noise characteristics.

This application note outlines some of the fundamental principles of synchronous AM detectors, and gives design examples using the XR-2228 multiplier/detector IC in conjunction with the XR-215 and the XR-2212 monolithic PLL circuits.

PRINCIPLES OF OPERATION

The phase-locked loop AM detector circuits operate on the so-called "coherent AM detection" principle, where the amplitude modulated input signal is mixed with an unmodulated "coherent" carrier signal, and then low-pass filtered to produce the desired demodulated output signal. Figure 1 gives a simplified block diagram of such a detector system.

The amplitude-modulated input signal can be described by an expression of the form:

$$\text{Input Signal} = V_m(t) \cos \omega_0 t$$

where $V_m(t)$ is the modulated amplitude of the input signal and ω_0 is the input signal frequency expressed in radians/seconds. If this signal is linearly multiplied with an unmodulated signal which has the same frequency and phase as the input signal then the output of the multiplier, $V_0(t)$, is a composite signal of the form:

$$V_0(t) = K_0 V_m(t) [1 + \cos (2 \omega_0 t)]$$

where K_0 is the gain of the multiplier circuit. If the above signal is then passed through a low-pass filter, to eliminate the double-frequency term, the resulting output signal is:

$$V_{out} = \text{Output Signal} = K_0 V_m(t)$$

which corresponds to the detected AM information.

The phase-locked loop AM detectors also operate on a similar principle: the PLL is made to "lock" on the carrier frequency of the input AM signal; then the VCO output of the PLL will regenerate the unmodulated coherent carrier signal necessary for detection. When this signal is mixed with the input AM signal and the resulting composite signal is passed through a low pass filter, one obtains the demodulated output. Figure 2 gives a block diagram of such an AM detector system. Compared to the basic synchronous AM detector system of Figure 1, the phase-locked loop AM detector of Figure 2 also has one added feature: the output of the PLL control voltage (i.e., output of the PLL low-pass filter) can be used as an FM detector or a frequency discriminator. Thus, such a system is capable of simultaneous AM and FM detection. In other words, the frequency and the amplitude modulation information present on the input signal can be separately and simultaneously demodulated. The particular design and application examples given in this application note fall into this category.

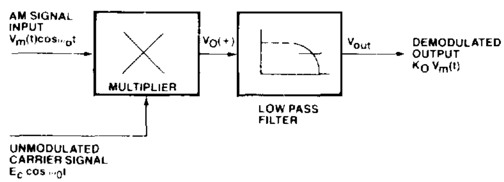

Figure 1. Block Diagram of a Synchronous AM Detector

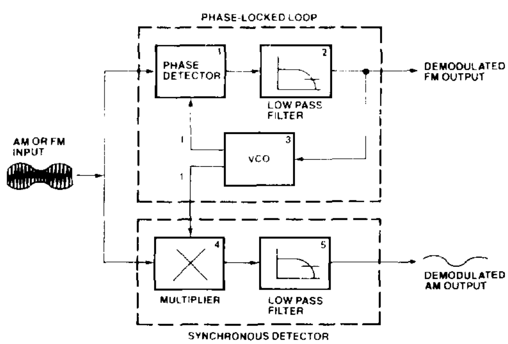

Figure 2. The Basic Phase-Locked Loop AM Detector

XR-2212 AND XR-2228 MONOLITHIC CIRCUITS

The XR-2212 monolithic PLL is made up of an input preamplifier, a phase-detector, a high-gain differential amplifier and a stable voltage-controlled oscillator (VCO) as shown in Figure 3. The key feature of the XR-2212 PLL is the temperature stability and the frequency accuracy of its VCO section; it offers 20 ppm/°C typical temperature stability and a frequency accuracy of ±1% for an external RC setting. The oscillator section of the XR-2212 contains a separate "quadrature output" terminal (Pin 15) which is particularly intended for interfacing with a synchronous AM detector such as the XR- 2228.

The XR-2228 multiplier/detector IC is specifically intended as a basic building block for synchronous AM detection. It contains a four-quadrant analog multiplier and a high-gain op amp on the same chip, as shown in the functional block diagram of Figure 4.

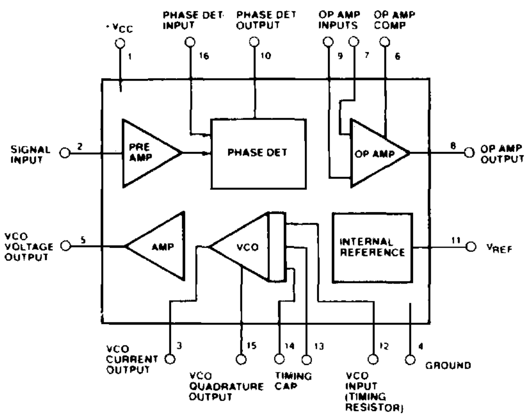

Figure 3. Functional Block Diagram of XR-2212 Precision Phase-Locked Loop

XR-215 HIGH FREQUENCY PHASE-LOCKED LOOP

The XR-215 is a high frequency phase-locked loop circuit capable operating with input signal frequencies up to 35MHz. It is comprised of a high frequency VCO, a phase-detector and an op amp section, as shown in the block diagram of Figure 5.

Unlike the XR-2212 PLL, the VCO section of the XR-215 does not have a separate quadrature output terminal. However, such a quadrature oscillator signal can be obtained by amplifying and "slicing" the triangle wave-form available across the timing capacitor (Pins 13 and 14) of the XR-215 oscillator section. Figure 6 shows the relative phase relationship of these oscillator wave-forms available from the circuit. The desired quadrature output signal (curve C of Figure 6) can be obtained by directly connecting one pair of the differential inputs of the XR-2228 directly across the timing capacitor terminals of the XR-215.

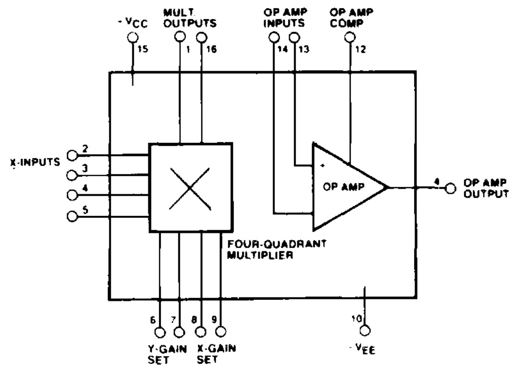

Figure 4. Functional Block Diagram of XR-2228 Multiplier/Detector IC

AM/FM DETECTION USING THE XR-2212 PLL

Figure 7 shows a generalized circuit connection diagram for a two-chip AM and FM detection system, utilizing the XR-2212 PLL and the XR-2228 multiplier/ detector. The XR-2212 section serves as the basic FM detector. The quadrature output of its VCO (Pin 15) is AC coupled to the Y input of the XR-2228.

The Y input of the XR-2228 is operated in its switching mode, with the Y gain terminals (Pins 6 and 7) shorted together. The AM and/or FM signal is simultaneously applied to both circuits through coupling capacitors; and all the mutiplier inputs are DC biased from the internal reference output of the XR-2212 (Pin 11). The output of the multiplier, at Pin 16, is AC coupled to the op amp section of the XR-2228, which serves as the post-detection amplifier for the demodulated AM signal.

The circuit configuration shown in Figure 7 can operate with a single power supply, over the supply voltage range, of 10V to 20V. Its operation or performance can be tailored for any particular AM and FM detection application by the choice external components shown in the figure, over a carrier frequency band of 1kHz to 300kHz. The functions of these external components are as follows:

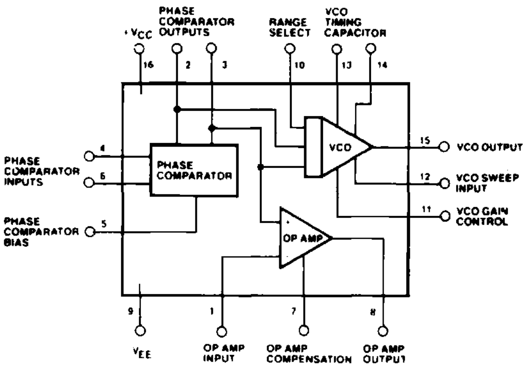

Figure 5. Functional Diagram of XR-215 High-Frequency Phase-Locked Loop

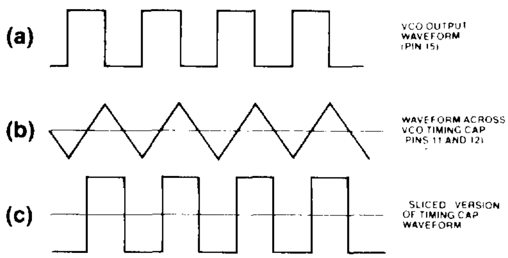

Figure 6. Timing Diagrams of VCO Output Waveforms from XR-215 Monolithic Phase-Locked Loop

a) R_0 and C_0 set the VCO center frequency for the XR-2212 PLL circuit. The center frequency, f_o, is given as:

$$f_0 = \frac{1}{R_0 C_0}$$

The VCO frequency f_0 is chosen to be equal to the carrier frequency of the input signal. R_0 is normally chosen to be in the range of 10kΩ to 100kΩ. This choice is arbitrary. For most applications $R_0 \approx 20k\Omega$ is recommended. Once f_0 is given and R_0 is chosen, the C_0 can be calculated from the above equation.

b) R_1 determines the tracking bandwidth of the PLL. For a required tracking bandwidth, Δf (see Figure 9 of XR-2212 data sheet) and f_o, R_1 can be calculated as:

$$R_1 = R_0 \frac{f_0}{\Delta f}$$

This tracking bandwidth, Δf, is the band of frequencies in the vicinity of f_o, over which the PLL can maintain lock.

c) C_1 sets the loop-damping factor for the PLL. For most applications, C_1 is chosen to be equal to one-half of C_o.

d) R_2 and C_2 form a low-pass filter for the detected FM signal. The 3dB frequencing, f_2, of this low-pass filter is:

$$f_2 = \frac{1}{2\pi R_2 C_2}$$

Normally, f_2 is chosen to be equal to the demodulated FM information bandwidth.

e) R_C and R_{F1} set the gain of the op amp section of the XR-2212 as:

$$A_V = 1 + \frac{R_{F1}}{R_C}$$

This op amp section serves as the post-detection amplifier for the demodulated FM signals.

f) R_X sets the multiplier gain for the X input and R_{F2} sets the gain of the op amp section of the XR-2228. Thus, the demodulated AM signal output swing, V_{out}, for a given input signal of peak amplitude of V_M and modulation index of m ($0 \le m \le 1$) can be approximated as:

$$V_{out} = \frac{(V_M)m}{4} \frac{R_{F2}}{R_X}$$

Thus, for example, a 100mV peak input signal with 30% AM modulation (m = 0.3) will give a demodulated output of 150mV peak, with R_{F2} = 100kΩ and R_X = 5kΩ, at Pin 11 of the XR-2228.

g) C_3, in conjunction with the 5kΩ internal impedance of the multiplier output (Pin 16) serves as the low-pass post-detection filter for the demodulated AM signal.

For further explanation and description for the system design equations, the reader is referred to the XR-2212 and the XR-2228 data sheets.

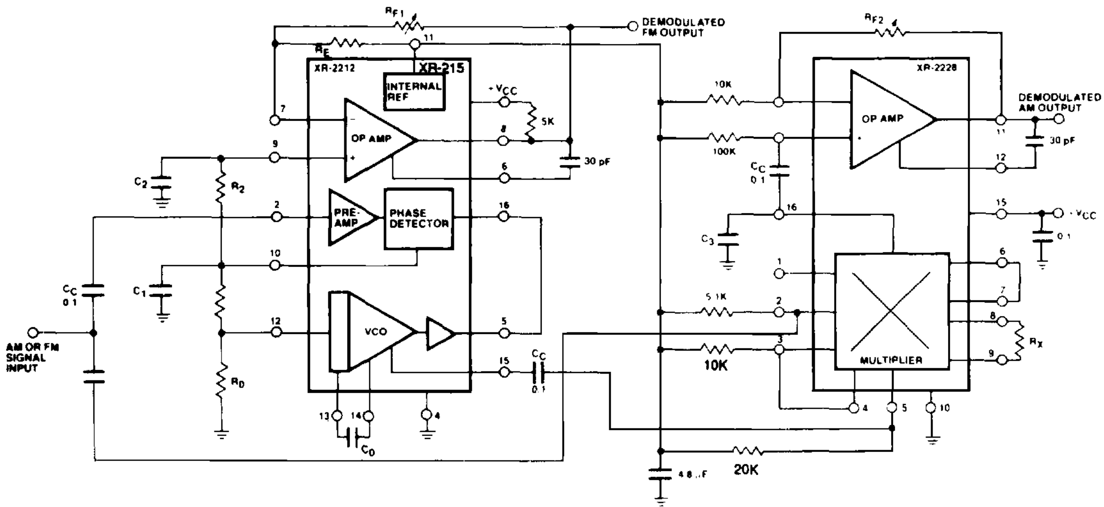

Figure 7. A Two-Chip AM/FM Detector System Using the XR-2212 Phase-Locked Loop and the XR-2228 Multiplier/Detector

Design Example

Design an AM demodulator for 100kHz carrier frequency with a detection (tracking) bandwidth of ±4%. The demodulated information bandwidth is 3kHz and an output level of one volt peak is required for a one volt peak input with 30% modulation.

Using the circuit of Figure 7, one proceeds as follows: Since FM detection is not required in this example, components R_2, C_2, R_C and R_{F1} are not essential to circuit operation. R_2 and R_C can be short-circuited, C_2 and R_{F1} can be left open-circuited. The rest of the component values are calculated as follows:

Step 1) Set $f_0 = 100kHz$ by choosing $R_0 = 20k\Omega$ and calculating C_0 from paragraph (a) above.

$$C_0 = \frac{1}{R_0 f_0} = 500pF$$

Step 2) Determine R_1 to set tracking bandwidth to ±4%, from paragraph (b): $R_1 = 500k\Omega$.

Step 3) Calculate C_1: $C_1 - C_0/2 \approx 250pF$.

Step 4) From paragraph (f), calculate the value of R_X and R_{F2}. For a typical choice of $R_X = 5k\Omega$, and $m = 0.3$ (30% modulation) with one volt input carrier level, the value of R_{F2} to get one volt demodulated output is: $R_{F2} = 67k\Omega$.

Step 5) Calculate C_3 to get 3kHz bandwidth for post-detection filter: $C_3 \approx 0.01\mu F$.

AM DETECTION USING THE XR-215 PLL

Figure 8 shows the circuit connection diagram for a two-chip AM and FM detection system, using the XR-215 high-frequency PLL in conjunction with the XR-2228 multiplier/detector. Because of the high-frequency capability of the XR-215, the circuit of Figure 8 is useful as a phase-locked AM detector for carrier frequencies up to 20MHz, and operates over a supply voltage range of 10V to 20V.

The VCO section of XR-215 does not have a separate quadrature output. However, this problem can be overcome by driving the XR-2228 multiplier directly from the timing capacitor terminals (Pins 13 and 14) of XR-215. The Y input of the XR-2228 is operated with maximum gain, since the Y gain control terminals (Pins 6 and 7) are shorted together. This causes the triangular waveform across C_0 to be converted to an effective quadrature drive as indicated by the timing diagram of Figure 6. The modulated input signal is simultaneously applied to both circuits through coupling capacitors. The phase-detector inputs of the XR-215, as well as the multiplier X inputs of the XR-2228, are biased at approximately one-half of V_{CC}, by means of an external resistive divider.

In Figure 8, C_0 sets the VCO frequency of the XR-215. In the case of FM demodulation, R_1 and C_1 serve as the post-detection filter for the detected FM signal and R_{F1} sets the gain of the FM post-detection amplifier.

The mode of operation of the XR-2228 is virtually the same as that described in connection with Figure 7: R_X sets the multiplier demodulation gain; C_3 serves as the low-pass post-detection filter. The values of R_X, R_{F2} and C_3 are calculated as given in paragraphs (f) and (g).

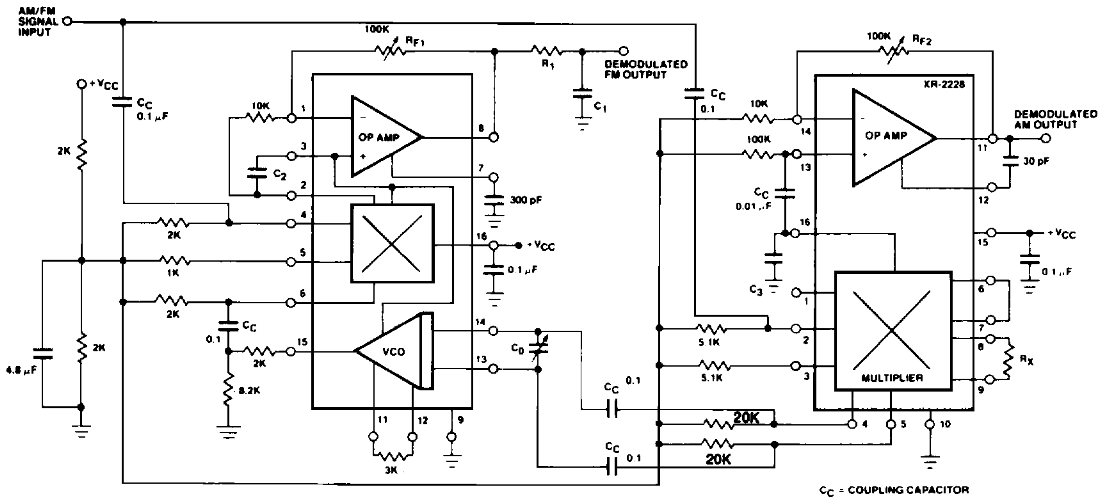

Figure 8. Circuit Connection for a High-Frequency AM and FM Detector Using the XR-215 and XR-2228