THE COSTAS LOOP

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ACHIEVEMENTS: *using the Costas loop for carrier acquisition from, and demodulation of, a DSBSC signal.*

PREREQUISITES: *familiarity with the quadrature modulator (as, for example, in the experiment entitled* ***Phase division multiplex,*** *in this Volume, would be an advantage.*

ADVANCED MODULES: *BIT CLOCK REGEN and SPECTRUM UTILITIES are both optional.*

EXTRA MODULES: *a total of three MULTIPLIER, two PHASE SHIFTER, and two TUNEABLE LPF modules.*

PREPARATION

the basic loop

Read about the Costas loop in your text book.

This loop, and its variations, is much-used as a method of carrier acquisition (and simultaneous message demodulation) in communication systems, both analog and digital.

It has the property of being able to derive a carrier from the received signal, even when there is no component at carrier frequency present in that signal (eg, DSBSC). The requirement is that the amplitude spectrum of the received signal be symmetrical about this frequency.

The basic Costas loop is illustrated in Figure 1.

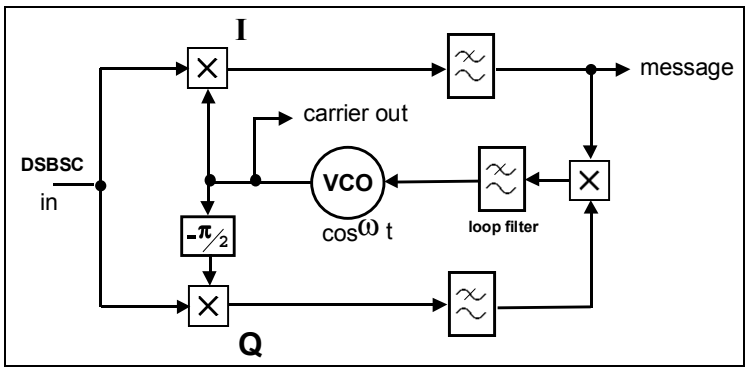

Figure 1: the Costas loop

The Costas loop[1] is based on a pair of quadrature modulators - two multipliers fed with carriers in phase-quadrature. These multipliers are in the in-phase (I) and quadrature phase (Q) arms of the arrangement.

Each of these multipliers is part of separate synchronous demodulators. The outputs of the modulators, after filtering, are multiplied together in a third multiplier, and the lowpass components in this product are used to adjust the phase of the local carrier source - a VCO - with respect to the received signal.

The operation is such as to maximise the output of the I arm, and minimize that from the Q arm. The output of the I arm happens to be the message, and so the Costas loop not only acquires the carrier, but is a (synchronous) demodulator as well.

A complete analysis of this loop is non-trivial. It would include the determination of conditions for stability, and parameters such as lock range, capture range, and so on. A simplified analysis is given in Appendix 1 to this experiment.

phase ambiguity

Although the Costas loop can provide a signal at carrier frequency, there remains a 180^0 phase uncertainty.

A phase ambiguity of 180^0 in many (typically analog) situations is of no consequence - for example, where the message is speech. In digital communications it will give rise to data inversion, and this may not be acceptable - but there are methods to overcome the problem.

See Tutorial Question Q9.

experiment philosophy

In most of the experiments involved with demodulation a stolen carrier is used. This allows full attention to be paid to the performance of the demodulator. Considerations of how to acquire a carrier from the received signal are ignored.

In this experiment, following a similar principle, attention will be paid to the means of acquiring a carrier from a DSBSC signal, without paying attention to the subsequent performance of the device for which the carrier is required (eg, a demodulator).

However, you could combine the two if you like.

measurements

The experiment to follow is described in outline only. It will take you only to the point at which the carrier is acquired.

Thus, before the experiment, you should prepare a list of those performance attributes with which you may be interested, with some suggestions as to how these might be measured.

[1] Costas, J.P. 'Synchronous Communications'. Proc.IRE, **44**, pp1713-1718, Dec.1956

EXPERIMENT

setting up the Costas loop

T1 *obtain a DSBSC signal. There should be one or more at TRUNKS, each based on a carrier at or near 100 kHz. Alternatively, if you have a fourth MULTIPLIER module, you could generate your own.*

For the Costas loop:

1. use TUNEABLE LPF modules for the filters in the I and Q arms. Set them both to their WIDE range, and TUNE them to their widest bandwidth.
2. use the RC LPF in the UTILITIES module to filter the control signal to the VCO (although you might find the LOOP FILTER in a BIT CLOCK REGEN module to be preferable).
3. before patching in the PHASE SHIFTER set the on-board toggle switch to the HI range. Then set it to approximately 90^0 using a 100 kHz sine wave.
4. before inserting the VCO set the on-board FSK/VCO switch to VCO. Select the HI frequency range with the front panel toggle switch.
5. if making your own DSBSC use an AUDIO OSCILLATOR for the message. You will find the loop will lock using any frequency within the tuning range, but for measurement purposes something well above the cut-off of the RC filter may be found more convenient.

T2 *model the Costas loop of Figure 1. A suitable model is shown in Figure 2.*

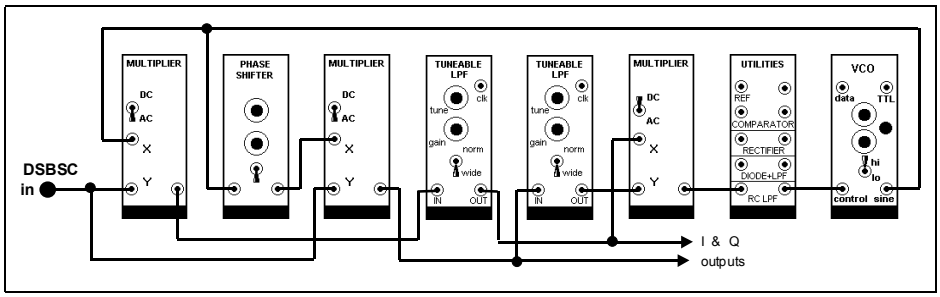

Figure 2: model of the Costas loop of Figure 1

T3 *look for a DSBSC signal at TRUNKS. If there is more than one, select one based on a 100 kHz carrier (**hint**: examine it with one arm of the Costas loop, with a stolen 100 kHz carrier from the TIMS MASTER SIGNALS module).*

T4 *check the amplitudes at all module interfaces. Check the gain of the TUNEABLE LPF modules in the I and Q arms so that the third MULTIPLIER is not overloaded (will the input amplitudes to this module change between the lock and not-locked condition ?).*

It is now time to lock the loop to the carrier of the incoming signal. There are various techniques to be adopted in the laboratory (where a reference carrier is available) while performing the alignment technique described in the next Task. Two of these are:

1. watch the reference carrier and the VCO on two channels of the scope.
2. watch the outputs of the filters in the I and Q arms.

Make your choice. Then:

T5 *synchronise the oscilloscope to either the reference carrier, or the output of the I channel, according to whichever of the above options you have chosen.*

T6 *disable the feedback loop by turning the GAIN of the VCO fully anti-clockwise.*

T7 *tune the VCO to within a few hundred Hertz (preferably less !) of 100 kHz, using the FREQUENCY COUNTER.*

T8 *slowly increase the VCO GAIN until the VCO locks to the DSBSC carrier, as indicated by the oscilloscope traces becoming stationary with respect to each other* ***or*** *by observing that the FREQUENCY COUNTER now reads 100.000 kHz.*

T9 *observe the demodulated output from the filter of the I arm. If lock has been achieved, but the demodulated waveform (the message) is other than sinusoidal, fine tune the VCO while still locked. The frequency won`t change (it is locked to the carrier) but this will result in a 'cleaner' and smaller control signal to the VCO, and a maximum amplitude minimum-distortion demodulated output.*

You will notice that lock is achieved when the VCO GAIN setting is above a certain minimum value. If the gain is increased 'too far', the lock will eventually be lost. From the behaviour of the VCO output signal (or otherwise) during this procedure, can you explain the meaning of 'too far' ?

T10 *open and close the connection from the DSBSC signal to the input of the Costas loop, and show that carrier acquisition is lost and regained. Although lock may appear to happen 'instantaneously' it will in fact take a finite number of carrier cycles after the connection is made. Note that the phase difference between the reference and recovered carrier takes one of two values, 180^0 apart. This phase ambiguity of the acquired carrier is associated with many carrier acquisition schemes.*

T11 *examine the other DSBSC at TRUNKS (if any). If they are not based on a 100 kHz carrier you will have to plan a different approach than the one suggested above. How will you know when lock has been achieved ?*

measurements

There are many measurements and observations that could now be made. This will depend upon the level of your course work.

Of practical interest would be a knowledge of the loop acquisition time under different conditions, lock range, holding range, conditions for stability, and so on. These dynamic measurements require more sophisticated instrumentation than you probably have.

Thus it is suggested that you confine your observations to checking that the loop actually works (already done), and some less sophisticated measurements.

VCO simulation

A technique of interest is to replace the VCO signal with a 'stolen' carrier connected, via a PHASE SHIFTER, into the loop. This simulates the locked VCO [2], and allows static observations of all points of the loop for various values of the phase angle α.

> *Appendix A to this experiment gives an **exact analysis** of this condition.*

In particular, the control signal to the VCO can be monitored.

You are looking for the condition where the magnitude of the control signal is a minimum. This must be the condition when final lock is achieved, since any other value would tend to move the VCO until it was met.

It is best to use a message frequency as high as possible so as not to confuse the measurement of the DC control signal with the unavoidable unwanted terms.

The analysis shows that every time a signal is processed by a multiplier followed by a filter there is an amplitude reduction of the signal under observation of one half due to the analytic process, and a further half due to the 'k factor' of each TIMS

[2] you may not agree with this !

MULTIPLIER module. Squaring the message introduces another reduction of one half.

Remember, then, that you will be looking for quite small signals, especially the DC control to the VCO.

This can be measured very conveniently with the SPECTRUM UTILITIES module. This is a meter which responds to DC or slowly-varying AC. Refer to the *Advanced Modules User Manual* for more details.

Your measurements under these conditions will confirm the predictions of the analysis. You could show that:

1. the message appears at the output of both the I and Q lowpass filters.
2. the AC term, at the output of the third multiplier, before removal by filtering, is at twice the message frequency
3. by adjusting the phase α until the DC from the filter at the output of the 'third' multiplier is reduced to zero,
    a) the I-filter output is maximized
    b) the Q-filter output is minimized (see Tutorial Question Q8)

TUTORIAL QUESTIONS

Q1 *a Costas loop can acquire a carrier from a received signal which itself contains no term at carrier frequency. Describe another scheme which can do this.*

Q2 *what are the required properties of the lowpass filter from which the VCO control signal is output ?*

Q3 *what properties of the Costas loop differentiate it from the phase locked loop ?*

Q4 *do any of the multipliers in a Costas loop need to be DC coupled ?*

Q5 *if you have achieved lock, it will be regained if:*

a) the inputs to the I and Q filters are swapped

b) the outputs from the I and Q arms are swapped

What will happen to the I and Q outputs in each case ?

Q6 *what would happen if the polarity of the control signal to the VCO is reversed ?*

Q7 *would you anticipate any differences in performance if the sinusoidal message was replaced with speech ?*

Q8 *if you used a filter from the 100 kHz CHANNEL FILTERS module to simulate a channel (for added realism) you may have had difficulty in achieving a deep null from the output of the Q-filter. How could this be ?*

Q9 *in a digital communications system the phase ambiguity introduced by a Costas loop for carrier acquisition need not necessarily be unacceptable. For example,*

a) some line codes would not be affected.

b) a training sequence may be used.

Explain.

Q10 *in the block diagram of Figure 1 there is a phase shifter of 90^0 ($\pi/2$). How would the performance of the loop be affected if this was set to 80^0 ?*

APPENDIX A

a simplified analysis

A simplified analysis of the Costas loop (Figure 1) starts by assuming that a stable lock has already been achieved.

This in turn assumes that the VCO is operating at the correct frequency, but that its relative phase is unknown. Call the angle α the phase difference between the received carrier and the VCO.

Let the received DSBSC be derived from the message m(t), and based on a carrier frequency of ω rad/s. This then is also the frequency of the VCO when locked.

The 'k (= ½) factor' of the TIMS MULTIPLIER modules has been included.

Define the signals into the multipliers of the I and Q arms as I and Q. Then:

$$I = m(t).k.\cos\omega t.\cos(\omega t + \alpha) \quad \text{..... A-1}$$

$$Q = m(t).k.\cos\omega t.\sin(\omega t + \alpha) \quad \text{..... A-2}$$

Equations (A-1) and (A-2) may be expanded, and only the low frequency terms retained, to obtain the signals from the lowpass filters. These go into the 'third' multiplier. Let these be named I_{LF}: and Q_{LF}. Then:

$$I_{LF} = ½.m(t).k.\cos\alpha \quad \text{..... A-3}$$

$$Q_{LF} = ½.m(t).k.\sin\alpha \quad \text{..... A-4}$$

After these are multiplied together, the output of the 'third' multiplier is:

$$\textit{'third' mult out} = ½.¼.m^2(t).k^2.\sin 2\alpha \quad \text{..... A-5}$$

No matter what the message m(t), the square of it will be positive, and contain a DC component, which can be filtered off.

If the message is a sine wave, and the DSBSC amplitude is unity, then:

$$\textit{filter output} = \frac{1}{16}k^2\sin 2\alpha. \quad \text{..... A-6}$$

The DC from the filter has a magnitude which is a function of the phase error α. This DC is the control signal to the VCO. It can change sign, according to the magnitude of α. Providing the loop is stable the tendency will be to shift the phase of the VCO until α is reduced to zero, since only then will the VCO come to rest.

message output

The message appears at the output of each of the I and Q filters. But under lock condition the phase error α will be zero, and eqns. A-3 and A-4 tell us that the message amplitude at the output of the I filter will be maximized, and minimized at the output of the Q filter.