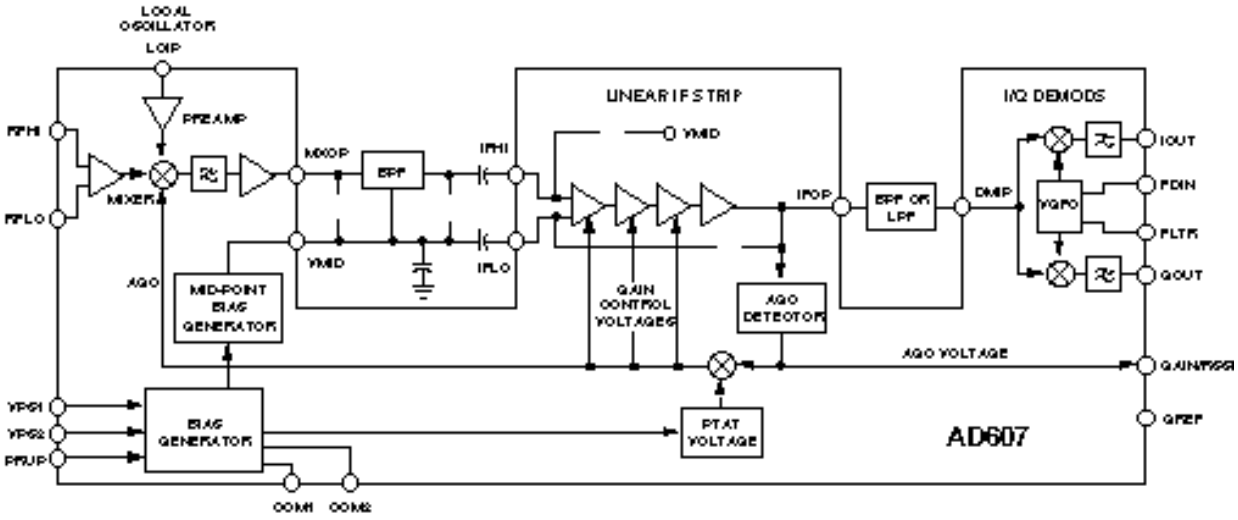
AD607 Architecture

The AD607 comprises a mixer with a LO preamp, a linear IF strip with voltage-controlled gain, dual (I & Q) demodulators, each followed by a 2-pole, 3-MHz low-pass filter, and a phase-locked voltage-controlled quadrature oscillator to provide the in-phase and quadrature clocks, as well as an on-board peak detector and AGC loop with a received-signal strength (RSSI). The IF strip's output is available for insertion of a low-pass or bandpass filter for noise reduction and/or an A/D for direct digitizing, as in Figure 1.



The signal path begins with the mixer. Although most IFs are in the 45 to 300-MHz range, it can accept inputs as high as 500 MHz. Its input-referred 1-dB compression point is -15 dBm (or ±54 mV, regardless of input termination) and its input third-order intercept point (IIP3) is -8 dBm. Both are measured with a 50-Ohms source and 50-Ohms input termination.

The mixer provides a high-impedance current output to drive a parallel-terminated filter; this avoids a 6-dB (voltage-mode) series termination loss. The conversion gain is specified for operation into an IF band-pass filter (BPF) load of 165 Ohms, i.e., a 330-Ohms filter doubly shunt-terminated and assuming a local oscillator drive at LOIP of at least -16 dBm (±50 mV, regardless of input termination). The IF signal voltage at pin MXOP can swing 2 V p-p when using a 3-V supply; the high headroom minimizes the likelihood of significant intermodulation from adjacent-channel and other strong interfering signals at the mixer output.

Both the mixer's conversion gain and the IF amplifier gain (dB) are proportionally controlled by the voltage, V(G), at pin GAIN/RSSI. The gain of all sections is maximum when V(G) is zero, and decreases, reaching a minimum at [V(P) - 0.8 V], where V(P) is the supply voltage; for example, V(G) = 2.2 V for V(p) = 3 V. Gain-control scaling is proportional to a reference voltage applied to GREF; when GREF is at the mid-point of the supply (VMID), the scale is nominally 20 mV/dB, or 50 dB/V.

Pin GAIN/RSSI, as an output, provides an RSSI voltage derived from the IF peak detector's output voltage; as in input, it accepts an external gain control voltage. In either case, the gain-

control voltage to the IF amplifier cells is multiplied by a voltage proportional to absolute temperature (PTAT) so that the overall gain scale-factor is insensitive to temperature.

Low-impedance IF output, IFOP, may be loaded by resistances as low as 500 Ohms to VMID. This output can either be digitized by an external A/D converter, as in Figure 1, or routed to the on-chip demodulator (DMIP) via a low-pass or bandpass filter to attenuate wideband noise generated in the high-gain IF amplifiers. For example, a single-pole low-pass filter at the IF reduces the signal level by 3 dB, but it improves the S/N ratio by reducing the wideband noise presented to the demodulator. Each demodulator comprises a full-wave synchronous detector and a two-pole low-pass filter, producing single-sided outputs at IOUT and QOUT.

The I and Q demodulators are driven by quadrature signals provided by an on-chip phase-locked loop (PLL)with its reference (at pin FDIN) at the IF.

The PLL's variable-frequency quadrature oscillator (VFQO) ensures excellent phase accuracy, as well as low EMI and power consumption. The PLL uses a sequential-phase detector (SPD), implemented in low-power current-mode logic, and a charge pump, which can source or sink 40 µA. The VFQO control path is filtered using an external CR network connected to FLTR. The circuit is designed to hold the frequency-control voltage on this pin for rapid reacquisition after power-down.

**The phase distortion introduced by the Chebyshev filter may be a problem in systems without some form of equalization.*